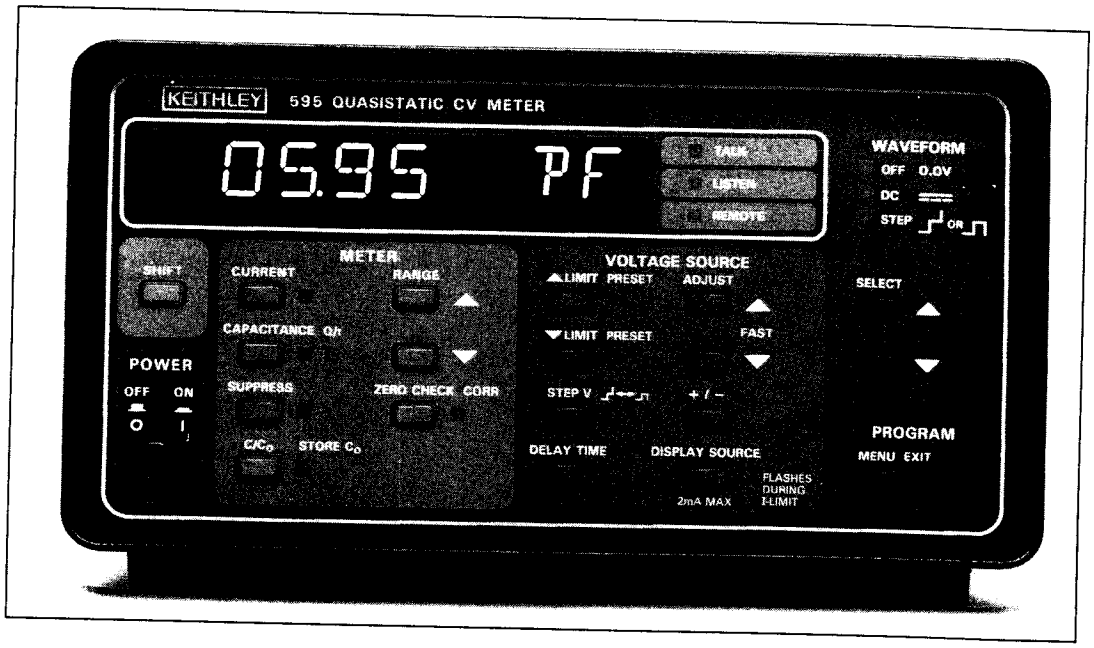
Quasistatic C-V Meter



- Measures quasistatic capacitance (10fF–20nF) and DC current (1fA–200μA)
- Correction of capacitance readings for background leakage currents
- Rapid assurance of device equilibrium
- Superior signal-to-noise performance, even with the slow voltage sweeps required by today's state-of-the-art devices.

IEEE-488

The Keithley 595 Quasistatic C-V Meter measures quasistatic capacitance versus voltage (C-V) characteristics of MIS semiconductor devices. The new C-V measurement technique used by the 595 provides diagnostics and correction for common sources of errors to increase confidence in test results.

Its current function serves as a sensitive picoammeter, directly measuring DC currents to 1fA. The built-in ±20V voltage source with DC, staircase, and squarewave waveforms permits both current and quasistatic capacitance measurements to be made either at a single device bias or as a function of voltage. This measurement flexibility makes the 595 appropriate for characterization of many semiconductor materials and components.

Quasistatic C-V measurements in the 595 are made using the "feedback charge" technique. Use of this technique makes it easy to measure quasistatic C-V characteristics of devices that would be unsuitable for testing with the traditional ramp method and static or Q-V methods.

Feedback charge brings to the 595:

- The ability to detect and correct for device or fixture leakage currents
- Rapid and quantitative indication of device equilibrium
- Superior signal-to-noise performance—even with the slow voltage sweeps required by today's state-of-the-art devices.

Applications

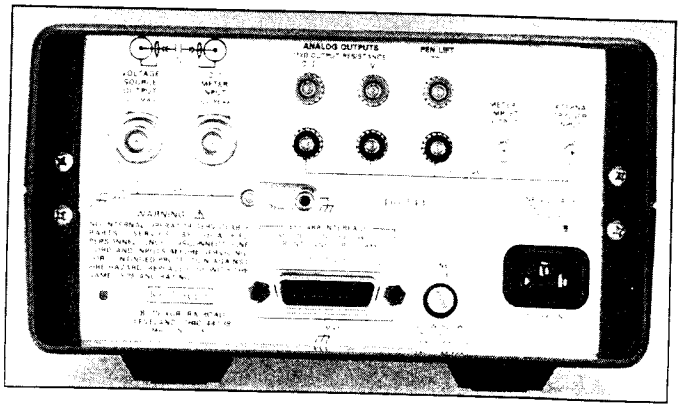
Quasistatic C-V measurements are commonly applied to characterize Metal-Insulator-Semiconductor (MIS) devices. They are used in the measurement of interface trap density and doping profiles corrected for the presence of interface traps. Quasistatic C-V is also used to measure mobile ion density by the triangular voltage-sweep method.

Measurements made with the 595 agree with quasistatic C-V results obtained using the ramp technique on silicon MOS devices. But the unique leakage correction capability of the feedback charge technique permits measurement of less-ideal MIS devices such as those based upon silicon carbide, GaAs, HgCdTe, InP, and compound insulators.

The Feedback Charge Method

The feedback charge method is based upon a staircase/squarewave voltage source and a charge measurement circuit, each connected to one terminal of the DUT.

Unlike other charge measurement techniques used for quasistatic C-V measurement, the feedback charge method presents a low impedance at the sensitive charge-measuring node. That reduces the otherwise extreme requirement for high shunt resistance and low shunt capacitance in device connections and further improves measurement integrity.



595
Quasistatic C-V Meter with two Model 4801 Low Noise BNC Input Cables

This product is available with an **Extended Warranty**. See page 221 for complete ordering information, or call 1-800-552-1115 (U.S. only).

CABLES

4801	Low Noise BNC Input Cable, 1.2m (4 ft.)
4803	Low Noise Cable Kit
7007-1	Shielded IEEE-488 Digital Cable, 1m (3.3 ft.)
7007-2	Shielded IEEE-488 Digital Cable, 2m (6.6 ft.)

CALIBRATION

5955	Calibration Capacitor Set

SOFTWARE

5956	Simultaneous C-V Software (for HP computers)
5957	Simultaneous C-V Software (for DOS computers)

RACK MOUNT KITS

1019A-1	Single Fixed Rack Mount Kit
1019A-2	Dual Fixed Rack Mount Kit
1019S-1	Single Slide Rack Mount Kit
1019S-2	Dual Slide Rack Mount Kit

See page 163 for descriptions of all accessories.

Quasistatic C-V Meter

To automate quasistatic C-V measurements use the 595 in a Model 82, 82-DOS, or 82-PS/2 System.

The voltage source outputs a small voltage step across the DUT, V_{STEP}, as part of either a squarewave or staircase waveform. This voltage step stimulates a displacement charge step in the device capacitance. The charge measurement circuit samples the device charge waveform before and after the stimulated charge step to determine Q_{STEP} and calculates the apparent device capacitance using the relation:

$$C_X = Q_{STEP} / V_{STEP}$$

The slope of the charge versus time waveform after the step, called Q/t, is also measured as an indication of the current flowing through the device at the time of measurement.

In an ideal capacitor, the Q/t current would always be zero since the displacement charge step would be transferred instantaneously at the time of the voltage step and no current would flow in the DUT thereafter in response to the DC voltage bias.

However, in practical devices this is seldom the case and Q/t is used to diagnose device or test error conditions such as:

- Constant leakage current resulting from humidity or electrochemical contamination.
- Parallel leakage resistance due to a leaky MIS device insulator or oxide.
- Non-equilibrium device settling current when the test voltage is swept too quickly.[1]

The 595 can also be used with the squarewave test signal waveform with a sequence of successively longer delay times to identify the test conditions required to achieve device equilibrium in a fraction of the time of other methods. When the measured capacitance saturates to C_{OX} and Q/t stabilizes at the constant leakage current value, the delay time is sufficient for device equilibrium.

Enhancing Measurement Integrity

The 595 has a choice of three non-recursive digital filters which can significantly reduce noise without shifting or distorting the quasistatic C-V curve. They can also be used to reduce measurement noise when measuring steady-state capacitances or currents.

Capacitance readings may be normalized to a stored value of C_O to eliminate the effects of gain errors and ease comparison of results from devices of different sizes.

The effects of current or capacitance offsets may be eliminated using Suppress, which subtracts a designated on-range reading from subsequent readings. Suppress is also useful for measuring relative to a fixed baseline.

FIGURE 1: 595 C vs. V and Q/t vs. V Curves Q/t used to indicate the degree of equilibrium

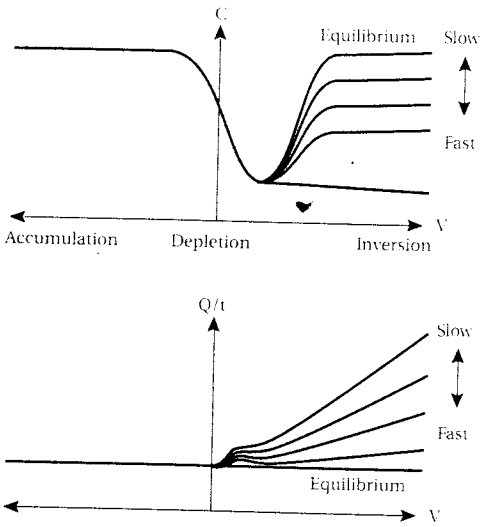
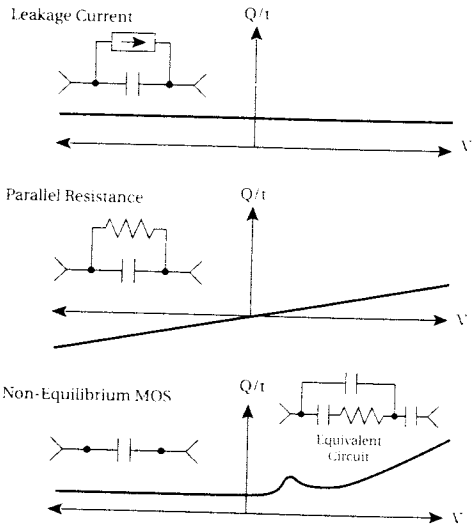


FIGURE 2: Q/t vs. V Curves used to diagnose leakage currents, parallel resistance, or non-equilibrium MOS conditions



Built-In Plotter Driver

You don't need to tie up a computer to make quasistatic C-V, Q/t, or I-V plots with the Model 595. It uses the IEEE-488 bus port to drive an HPGL plotter. No software or computer is needed. The 595 also outputs X-Y graphs with pen control to analog plotters.

[1]The Model 595 may be used for conventional quasistatic C-V testing in which the test voltage is swept from inversion to accumulation in non-equilibrium. However, results obtained under these conditions should be verified against results of equilibrium tests to ensure that interface trap measurements are not adversely affected.

Quasistatic C-V Meter 595

IEEE-488 BUS IMPLEMENTATION

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, UNL, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

PROGRAMMABLE PARAMETERS: Function, RANGE, ZERO CHECK, CORRect, SUPPRESS, C/C_O, STORE C_O, Voltage Source Parameters, WAVEFORM, Display Parameter, Filter, Trigger, Analog Output ×10, PEN LIFT, Capacitance Correction, Calibration, Self Test, Output Format, SRQ, Status, ASCII Terminator, EOI.

PLOTTER: Controls HP 7470A plotter or equivalent using HPGL via IEEE-488 for real time plotting of C, Q/t, or I vs. V curves. Accessed by selecting Model 595 address 42 or 43. Talks to plotter on address 05. HPGL® commands used are IN, IP, IW, PA, PD, PU, SC, SI, SP.

GENERAL

DISPLAY: 4½-digit numeric LEDs with appropriate decimal point and polarity indication. Signed 2-digit alphanumeric exponent.

UPDATE RATE: In I, one reading each Step Time. In C, one reading each 2× Step Time.

OVERRANGE INDICATION: Display reads OL.

INPUT BIAS CURRENT (all functions): <5fA (5×10^{-15}A) at 23°C after warm-up. Approximately doubles for every 10°C increase in ambient temperature above 23°C.

INPUT VOLTAGE BURDEN: <1mV.

MEASUREMENT SETTLING TIME: Within one reading except 2.5 s (to 1% of step change) on pA ranges.

PROGRAMS: Provide front panel access to Filter, Trigger, Analog Output ×10, Corrected Capacitance, IEEE-488 address, Alpha or Numeric Exponent, plotter Y Hi Limit, Y Lo Limit, Grid, 50/60Hz selection, and Digital Calibration.

SUPPRESS: Allows zeroing of on-range C, C/C_O, or I readings. Allows relative readings to be made with respect to a baseline value.

FILTER:

Code	Readings Weighted	Typical White Noise Reduction	Typical Measurement Use
0	1	None	OFF
1	3	1.7	C or I vs. V
2	9	2.5	C or I vs. V
3	24	5	Steady C, I

MAXIMUM INPUT: 30V peak, DC to 60Hz sine wave.

MAXIMUM COMMON MODE VOLTAGE: 30V maximum, DC to 60Hz sine wave.

INPUT CONNECTOR: Isolated BNC on rear panel.

OUTPUT CONNECTORS: Isolated BNCs on rear panel for VOLTAGE SOURCE OUTPUT, EXTERNAL TRIGGER, and METER COMPLETE. 5-way binding posts on rear panel for ANALOG OUTPUTs, PEN LIFT, GUARD, and Chassis.

EXTERNAL TRIGGER: TTL compatible EXTERNAL TRIGGER and METER COMPLETE.

ENVIRONMENT: Operating: 0° to 40°C, relative humidity 70% non-condensing up to 35°C. **Storage:** –25° to +65°C.

WARM-UP: 2 hours to rated accuracy (see manual for recommended procedure).

POWER: 105–125V or 210–250V (internal switch selected), 50Hz to 60Hz, 15VA max. 90–110V and 180–220V version available upon request.

DIMENSIONS, WEIGHT: 127mm high × 216mm wide × 359mm deep (5 in. × 8½ in. × 14⅛ in.). Net weight 3.2kg (6 lbs., 14 oz.).

ACCESSORY SUPPLIED: Two Model 4801 Low Noise BNC Input Cables.

CAPACITANCE (C)

RANGE	RESOLUTION	ACCURACY* (1 Year) 18°–28°C ±(%rdg + counts)	MAXIMUM ALLOWABLE Q/t AT HALF RANGE C DELAY TIME=0.07s STEP V = 0.10V
200 pF	10 fF	1.0 + 10	90.00 pA
2 nF	100 fF	0.8 + 2	0.900 nA
20 nF	1 pF	0.6 + 2	9.000 nA

*Exclusive of noise, for STEP V ≥ 0.05V and DELAY TIME ≤ 1 second. For other parameters, derate by (5mV/STEP V) × (DELAY TIME/1 second) in pF at 23°C. Double the derating for every 10°C rise in ambient temperature above 23°C.

TYPICAL PEAK-TO-PEAK NOISE (with supplied cables): ±(0.015% rdg + 0.006pF) × (100mV/STEP V) ± 1 count with FILTER 2, 0.1Hz to 10Hz.

Q/t: Measures non-equilibrium current and leakage current in the device under test during a capacitance measurement.

Display: 3 digits typical; resolution from 0.01fA to 0.01nA per count depending on range, STEP V, and DELAY TIME.

Measurement Time: DELAY TIME/8 or 0.044s, whichever is greater. Sampled at the end of each capacitance measurement.

Accuracy (1 Year, 18°–28°C): ±(1.0% rdg + 2 counts) exclusive of input bias current and noise.

C/C_O: Outputs normalized reading (up to 1.9999) as a ratio of the measured capacitance to a user-stored value of C_O.

TEMPERATURE COEFFICIENT (0°–18°C & 28°–40°C): ±(0.02% rdg + 0.1 count)/°C.

CURRENT (I)

RANGE	RESOLUTION	ACCURACY (1 Year)* 18°–28°C ±(%rdg + counts)	TEMPERATURE COEFFICIENT 0°–18°C & 28°–40°C ±(%rdg + counts)/°C
20 pA	1 fA	1.5 + 14	0.15 + 3
200 pA	10 fA	1.5 + 2	0.15 + 0.3
2 nA	100 fA	0.25 + 6	0.015 + 3
20 nA	1 pA	0.25 + 1	0.015 + 0.3
200 nA	10 pA	0.1 + 4	0.01 + 3
2 µA	100 pA	0.1 + 1	0.01 + 0.3
20 µA	1 nA	0.1 + 4	0.01 + 3
200 µA	10 nA	0.1 + 1	0.01 + 0.3

*When properly zeroed.

NMRR: 70dB on pA ranges, 60dB on nA and µA ranges, at 50 or 60Hz ±0.1%.

VOLTAGE SOURCE (V)

OUTPUT: –20.00V to 20.00V in 0.01V increments.

ACCURACY (1 Year, 18°–28°C): ±(0.2% + 10mV).

TEMPERATURE COEFFICIENT (0°–18°C & 28°–40°C): ±(0.005% + 200µV)/°C.

MAXIMUM OUTPUT CURRENT: ±2mA; active current limit at <4mA with annunciation.

SETTLING TIME: <3ms to rated accuracy.

NOISE: <(1ppm of output voltage + 100µV) p-p from 0.1 to 10Hz.

STEP VOLTAGE: Selectable as 0.01V, 0.02V, 0.05V, or 0.10V (±2%). Polarity selectable + or –.

DELAY TIME: 0.07s to 199.99s in 0.01s increments (±0.05%).

STEP TIME: DELAY TIME plus 0.04s typical.

WAVEFORM:

OFF: Outputs 0.0V ±0.01V.
DC: Outputs the programmed voltage.
STEP: Outputs changes in increments of STEP V from programmed voltage in either staircase or squarewave.

SQUAREWAVE: Repeatedly toggles between the programmed voltage and the programmed voltage plus STEP V, dwelling at each level for Step Time.

STAIRCASE: Repeatedly increments the output by STEP V until the upper or lower LIMIT is reached, dwelling at each level for Step Time.

ANALOG OUTPUTS

C, I OUTPUT LEVEL: 1V = 10,000 counts on ×1 gain; 1V = 1000 counts on ×10 gain.

V OUTPUT LEVEL: 1V = 10V on voltage source output.

MAXIMUM OUTPUT VOLTAGE: ±2V.

OUTPUT RESISTANCE: 1kΩ.

ACCURACY: ±(0.25% of displayed reading + 2mV).

RESPONSE TIME: Follows display.

ISOLATION: 30V peak from chassis or GUARD to ANALOG OUTPUT LO, which is connected to IEEE COMMON.